



Substitute for form 1449A/PTO		Complete If Known			
		Application / Conf. No.	10/090,251 / 4101		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Filing Date	March 01, 2002		
		First Named Inventor	Warren E. Cory		
		Art Unit	2631		
		Examiner Name	Unknown		
Sheet	1	of	7	Attorney Docket Number	X-1045 US

U.S. PATENT DOCUMENTS						
Examiner Initials *	Cite No.¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)				
JL		US-	4,758,985	07-19-88	Carter	
		US-	5,142,625	08-25-92	Nakai	
		US-	4,855,669	08-08-89	Mahoney	
		US-	34,363	08-31-93	Freeman	RECEIVED
		US-	5,072,418	12-10-91	Boutaud et al.	
		US-	5,274,570	12-28-93	Izumi et al.	JAN 22 2004
		US-	5,550,782	08-27-96	Cliff et al.	
		US-	5,347,181	09-13-94	Ashby et al.	Technology Center 2600
		US-	5,339,262	08-16-94	Rostoker et al.	
		US-	5,311,114	05-10-94	Sambamurthy et al.	
		US-	5,504,738	04-02-96	Sambamurthy et al.	
		US-	5,552,722	09-03-96	Kean	
		US-	6,467,009	10-15-02	Young et al.	
		US-	5,914,616	06-22-99	Winegarten et al.	
		US-	5,457,410	10-10-95	Ting	
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		US-	5,581,745	12-03-96	Muraoka	
		US-	5,742,179	04-21-98	Sasaki	
		US-	5,600,845	02-04-97	Gilson	
		US-	5,574,930	11-12-96	Halverson Jr., et al.	

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		Country Code ³	Number ⁴ Kind Code ⁵ (if known)				
JL			EP 0315275 A2	10-05-89	LSI Logic		
			WO 93 25968 A1	12-23-93	Furtek		
			EP 0 905 906 A2	03-31-99	Lucént		
			EP 1 235 351 A1	08-28-02	Matsushita Electric		
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OTHER - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. 1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 2
J		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		VASON P. SRINI, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		JACOB DAVIDSON, "FPGA IMPLEMENTATION OF RECONFIGURABLE MICROPROCESSOR," IEEE, March 1993, pp. 3.2.1 - 3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		CHRISTIAN ISELI et al., "BEYOND SUPERSCALER USING FPGA's," IEEE, April 1993, pp. 486-490, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		P.C. FRENCH et al., "A SELF-RECONFIGURING PROCESSOR," IEEE, July 1993, pp. 50-59, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		Christian Iseli et al., "SPYDER: A RECONFIGURABLE VLIW PROCESSOR USING FPGA's," IEEE, July 1993, pp. 17-24, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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J		OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

Examiner Signature	<i>[Signature]</i>	Date Considered	09/27/05
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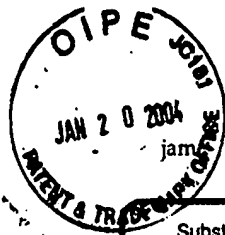
OTHER - NON PATENT LITERATURE DOCUMENTS			
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✓		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
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		YAMIN LI et al., "ALZUP-A PIPELINED PROCESSOR DESIGN & IMPLEMENTATION ON XILINX FPGA CHIP," IEEE, September 1996, pp 98-106, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		RALPH D. WITTIG et al., "ONECHIP: AN FPGA PROCESSOR WITH RECONFIGURABLE LOGIC," April 17, 1996, pp 126-135, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," January 27, 1999, Ch. 3, pp 3-1 TO 3-50, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
		WILLIAM B. ANDREW et al., "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
✓		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	

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		First Named Inventor	Warren E. Cory		
		Art Unit	2631		
		Examiner Name	Unknown		
Sheet	5	of	7	Attorney Docket Number	X-1045 US

U.S. PATENT DOCUMENTS						
Examiner Initials *	Cite No.†	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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JJ		US-	6,011,407	01-04-00	New	
		US-	6,172,990	01-09-01	Deb et al.	
		US-	10/001,871	11-19-01	Douglass et al.	
		US-	5,760,607	06-02-98	Leeds et al.	RECEIVED
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		US-	6,510,548	01-21-03	Squires	
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		US-	6,154,051	11-28-00	Nguyen et al.	
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		US-	6,356,987	03-12-02	Aulas	
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	JT		US-	6,272,451	08-07-01	Mason et al.

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Sheet	6	of	7
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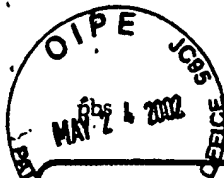
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JJ		US-	5,361,373	11-01-94	Gilson	
		US-	5,537,601	07-16-96	Kimura et al.	
		US-	5,652,904	07-29-97	Trimberger	
		US-	5,671,355	09-23-97	Collins	
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JT		US-	6,343,207 B1	01-29-02	Hessel et al.	
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OTHER -- NON PATENT LITERATURE DOCUMENTS

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